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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,481	10/02/2003	Shiao-Shien Chen	NAUP0549USA	2480

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AVC

Office Action Summary	Application No.	Applicant(s)	
	10/605,481	CHEN ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, and 3 thru 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soderbarg et al. 5,844,272 in view of Yu et al. 6,774,436 B1. Soderbarg discloses (see, for example, FIG. 4) a SOI transistor comprising a n- doped layer (well of first conductivity type) 21, thin film body, insulated substrate (support substrate) 50, thin insulator layer (gate dielectric layer) 26, extended gate layer (polysilicon gate) 30, n+ area (first gate section of first conductivity type) 34, p-doped body (extended well region) 22, p- area (second gate section of second conductivity type) 31, n+ source region 24, and n+ drain region 23. In column 3, lines 27-28, Soderbarg discloses the extended gate layer comprising polysilicon. Soderberg does not disclose a buried oxide layer. However, Yu discloses (see, for example, Fig. 1) a SOI transistor comprising a substrate 18, and a BOX layer (buried oxide layer) 16. The buried oxide layer provides a support for the SOI transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a buried oxide layer in order to provide a support for the SOI transistor.

Regarding claim 3, Soderbarg in view of Yu does not disclose said dielectric layer having a thickness of between about 5~120 angstroms. However, the thickness of said dielectric layer is a result effective variable that one of ordinary skill in the art would optimize for forming the

channel in a transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have said dielectric layer having a thickness of between about 5~120 angstroms because it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art (In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980) in order for one to form an adequate channel in a transistor.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soderbarg et al. '272 in view of Yu et al. '436 B1 as applied to claims 1, and 3-5 above, and further in view of Mistry et al. 5,821,575. Soderbarg in view of Yu does not disclose said gate dielectric layer being selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer. However, Mistry discloses (see, for example, column 5, lines 52-59) a semiconductor device comprising an electrical insulating layer (gate dielectric layer) 44 and a gate electrode 48. Mistry further discloses the electrical insulating layer being silicon dioxide. It would have been obvious to one of ordinary skill in the art at the time of invention to have said gate dielectric layer being selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer in order to have adequate insulation between the extended gate layer, and thin film body.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soderbarg et al. '272 in view of Yu et al. '436 B1 as applied to claims 1, and 3-5 above, and further in view of Ohyanagi et al. 6,657,257 B2. Soderbarg in view of Yu does not disclose said first conductivity

type being P type, and said second conductivity type being N type. However, Ohyanagi discloses (see, for example, column 3, lines 47-50) a semiconductor device wherein the semiconductor device may go from P-type to N-type by simply reversing the conductivity type of each semiconductor layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said first conductivity type being P type, and said second conductivity type being N type in order to form a semiconductor device of reverse conductivity type.

5. Claims 7, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Soderbarg et al. 5,844,272 in view of Kawanaka et al. 6,693,328 B1 in view of Kunikiyo 6,545,318. Soderbarg discloses (see, for example, FIG 6) a SOI transistor comprising a silicon wafer having a thin film body, insulation (gate dielectric layer), n+ extended gate layer (polysilicon gate of first conductivity type), p+/p- area (implanted with ions of second conductivity type), source region, and drain region. Soderberg does not disclose a supporting substrate, and a buried oxide layer. However, Kawanaka discloses (see, for example, FIG. 2A) a SOI transistor comprising a substrate (supporting substrate) 1, and insulating film (buried oxide layer) 2. The substrate and insulating film provide a support for the SOI transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a supporting substrate, and a buried oxide layer in order to provide a support for the SOI transistor.

Soderbarg does not disclose oxide filled trenches that extend downwards from said main surface as far as said buried layer, and a first end of said polysilicon gate over a first oxide filled trench across said well to a second end of said polysilicon gate over a second oxide filled trench.

However, Kawanaka discloses (see, for example, FIG. 2A) a SOI transistor comprising an element separating insulating film (filled trenches) 4, insulating film 2, and gate electrode G. Both ends of the gate electrode extend over the element isolating film 4. The element separating insulating film isolates the SOI transistor from other active devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have filled trenches that extend downwards from said main surface as far as said buried layer, and a first end of said polysilicon gate over a first filled trench across said well to a second end of said polysilicon gate over a second filled trench in order to isolate the SOI transistor from other active devices.

Soderbarg in view of Kawanaka does not disclose the first filled trench and second filled trench being oxide filled. However, Kunikiyo discloses (see, for example, Fig. 3) a SOI transistor comprising an isolation insulating film 4, buried oxide film 2, gate electrode 6. Both ends of the gate electrode extends over the isolation insulating film 4. In column 5, lines 11-12, Kunikiyo discloses the isolation insulating film comprising silicon oxide. The isolation insulating film adequately isolates the SOI transistor from other active devices. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the first filled trench and second filled trench being oxide filled in order to use material that adequately isolates the SOI transistor from other active devices.

Regarding claim 9, Soderbarg in view of Kawanaka in view of Kunikiyo does not disclose said dielectric layer having a thickness of between about 5~120 angstroms. However, the thickness of said dielectric layer is a result effective variable that one of ordinary skill in the art would optimize for forming the channel in a transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have said

dielectric layer having a thickness of between about 5~120 angstroms because it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art (In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980) in order for one to form an adequate channel in a transistor.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soderbarg et al. '272 in view of Kawanaka et al. '328 B1 in view of Kunikiyo '318 as applied to claims 7, 9, 10, and 12 above, and further in view of Mistry et al. 5,821,575. Soderbarg in view of Kawanaka in view of Kunikiyo does not disclose said dielectric layer being selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer. However, Mistry discloses (see, for example, column 5, lines 52-59) a semiconductor device comprising an electrical insulating layer (gate dielectric layer) 44 and a gate electrode 48. Mistry further discloses the electrical insulating layer being silicon dioxide. It would have been obvious to one of ordinary skill in the art at the time of invention to have said gate dielectric layer being selected from the group consisting of silicon dioxide, nitrogen contained silicon dioxide, oxynitride, and Al, Az, La, Ta, or Hf contained high K dielectric layer in order to have adequate insulation between the extended gate layer, and thin film body.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Soderbarg et al. '272 in view of Kawanaka et al. '328 B1 in view of Kunikiyo '318 as applied to claims 7, 9, 10, and 12 above, and further in view of Ohyanagi 6,657,257 B2. Soderbarg in view of Kawanaka

in view of Kunikiyo does not disclose said first conductivity type being P type, and said second conductivity type being N type. However, Ohyanagi discloses (see, for example, column 3, lines 47-50) a semiconductor device wherein the semiconductor device may go from P-type to N-type by simply reversing the conductivity type of each semiconductor layer. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have said first conductivity type being P type, and said second conductivity type being N type in order to form a semiconductor device of reverse conductivity type.

Response to Arguments

8. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
February 15, 2005

Tom Thomas

TOM THOMAS
SUPERVISOR [illegible] EXAMINER